Amendments to the Specification:

Please replace the paragraph beginning at page 3, line 1 with the following amended paragraph:

The local area network 13 may be coupled to a wide area network such as the Internet, through a gateway (not shown). The telephone system 10 also includes components 14, including a microphone 14a, speaker 14b and a handset 14c that are connected to the network processor 12 through a digital-to-analog/analog-to-digital (DA/AD) converter 22. The DA/AD converter 22 is connected to the network processor 12 via an integrated pulse code modulation (PCM) port 24 that is described in further detail below. Each of the PCM ports can handle up to 30 time slots with each slot capable of handling a 64K bit/sec voice channel. The PCM ports therefore serve as the interface between the internal hardware of the IP processor and a external peripheral. In addition to transmitting and receiving voice data, the telephone system also transmits and receives data from a workstation 18 that is connected to the network processor 12 through an Ethernet port 26. A second Ethernet port 28 is used to connect the network processor to the local area network 13.

C1

Please replace the paragraph beginning at page 3, line 31 with the following amended paragraph:

To connect the network processor directly to a local area network, the processor 12 includes a pair of IEEE 802.3 media access controllers and a repeater 40 in accordance with the IEEE standard.

C2

Please replace the paragraph beginning at page 3, line 34 with the following amended paragraph:

Each of the USB ports, 802.3 MACs and the PCM ports are connected to a flexible peripheral interconnect bus [[34]] 36 that is described in the specifications entitled "Flexible

C3

a3

Peripherals Interconnect Bus Version 3.2" and "BPI Specification Draft Version 0.9" as attached as Appendices C and D, respectively.

Please replace the paragraph beginning at page 4, line 26 with the following amended paragraph:

a4

A data management transmit and receive blocks 24a and 24b are connected to the FPI bus [[34]] 36 through a master/slave interface that is described in the specification entitled "Platform Concept: SMIF Specification Version 1.0" attached as Appendix O.

Please replace the paragraph beginning at page 4, line 31 with the following amended paragraph:

a5

The remaining components of the PCM port 24 are connected to the FPI bus [[34]] 36 through a BPI interface as described in "BPI Specification Draft Version 0.9" attached as Appendix P.